OptiMOS® Power-Transistor

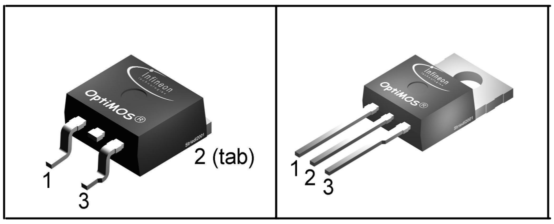
Feature

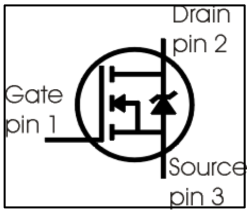
- N-Channel
- Enhancement mode
- Logic Level
- 175°C operating temperature
- Avalanche rated
- d*v*/d*t* rated

Product Summary

V_{DS}	55	V
$R_{DS(on)}$	7	mΩ
I_D	80	A

P- TO263 -3-2 P- TO220 -3-1





Type	Package	Ordering Code	Marking
SPP80N06S2L-07	P- TO220 -3-1	Q67040-S4285	2N06L07
SPB80N06S2L-07	P- TO263 -3-2	Q67040-S4288	2N06L07

Maximum Ratings, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current 1) T_C=25°C	I_D	 80 80	A
Pulsed drain current T_C=25°C	$I_{D\ puls}$	320	
Avalanche energy, single pulse I_D=80 A , V_{DD}=25V, R_{GS}=25Ω	E_{AS}	450	mJ
Repetitive avalanche energy, limited by T_{jmax} 2)	E_{AR}	21	
Reverse diode d*v*/d*t* I_S=80A, V_{DS}=44V, d*i*/d*t*=200A/µs, T_{jmax}=175°C	d*v*/d*t*	6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_C=25°C	P_{tot}	210	W
Operating and storage temperature	T_j , T_{stg}	-55... +175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	0.46	0.7	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	62	
@ 6 cm^2 cooling area 3)		-	-	40	

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage V_{GS}=0V, I_D=1mA	$V_{(BR)DSS}$	55	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ I_D=150µA	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}				µA
V_{DS}=55V, V_{GS}=0V, T_j=25°C		-	0.01	1	
V_{DS}=55V, V_{GS}=0V, T_j=125°C		-	1	100	
Gate-source leakage current V_{GS}=20V, V_{DS}=0V	I_{GSS}	-	1	100	nA
Drain-source on-state resistance V_{GS}=4.5V, I_D=60A	$R_{DS(on)}$	-	7.1	10	mΩ
Drain-source on-state resistance V_{GS}=10V, I_D=60A	$R_{DS(on)}$	-	5.6	7	

1Current limited by bondwire ; with an R_{thJC} = 0.7K/W the chip is able to carry I_D= 121A at 25°C, for detailed information see app.-note ANPS071E available at *www.infineon.com/optimos*

2Defined by design. Not subject to production test.

3Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

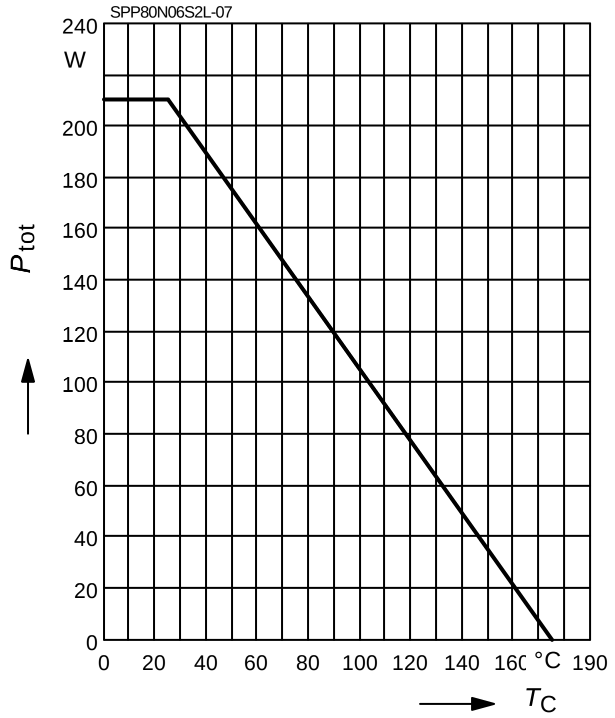
Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics						
Transconductance	g_{fs}	V_{DS}≥2*I_D*$R_{DS(on)max}$, I_D=80A	52	104	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	3160	4210	pF
Output capacitance	C_{oss}		-	740	990	
Reverse transfer capacitance	C_{rss}		-	210	310	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30V, V_{GS}=10V, I_D=80A, R_G=2Ω	-	18	27	ns
Rise time	t_r		-	35	52	
Turn-off delay time	$t_{d(off)}$		-	28	42	
Fall time	t_f		-	31	47	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=44V, I_D=80A	-	11	14	nC
Gate to drain charge	Q_{gd}		-	32	48	
Gate charge total	Q_g	V_{DD}=44V, I_D=80A, V_{GS}=0 to 10V	-	95	130	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=44V, I_D=80A	-	3.5	-	V
Reverse Diode						
Inverse diode continuous forward current	I_S	T_C=25°C	-	-	80	A
Inv. diode direct current, pulsed	I_{SM}		-	-	320	
Inverse diode forward voltage	V_{SD}	V_{GS}=0V, I_F=80A	-	0.9	1.3	V
Reverse recovery time	t_{rr}	V_R=30V, I_F=I_S, di_F/dt=100A/µs	-	59	75	ns
Reverse recovery charge	Q_{rr}		-	80	100	nC

1 Power dissipation

$P_{tot} = f(T_C)$

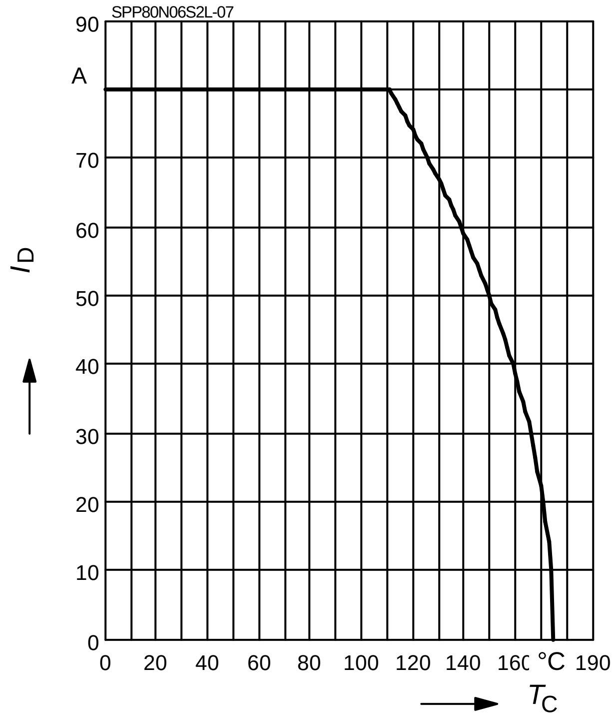
parameter: $V_{GS} \geq 4$ V



2 Drain current

$I_D = f(T_C)$

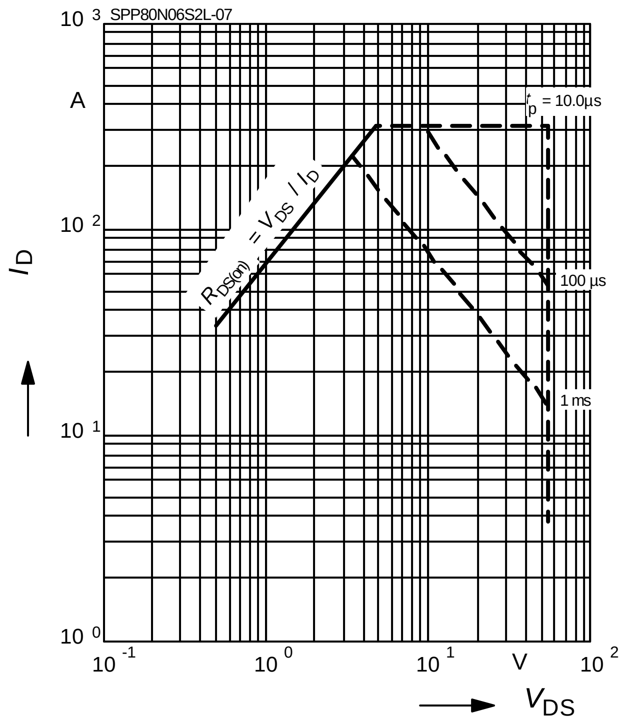
parameter: $V_{GS} \geq 10$ V



3 Safe operating area

$I_D = f(V_{DS})$

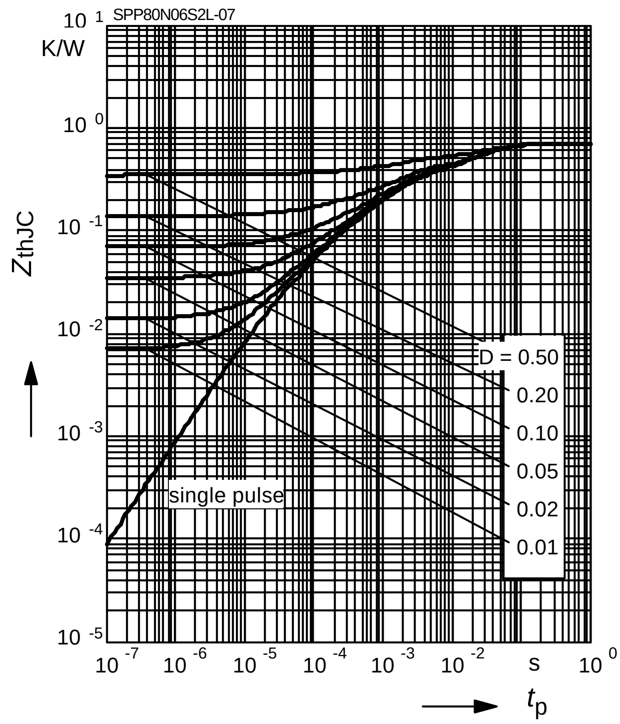
parameter : $D = 0$, $T_C = 25$ °C



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

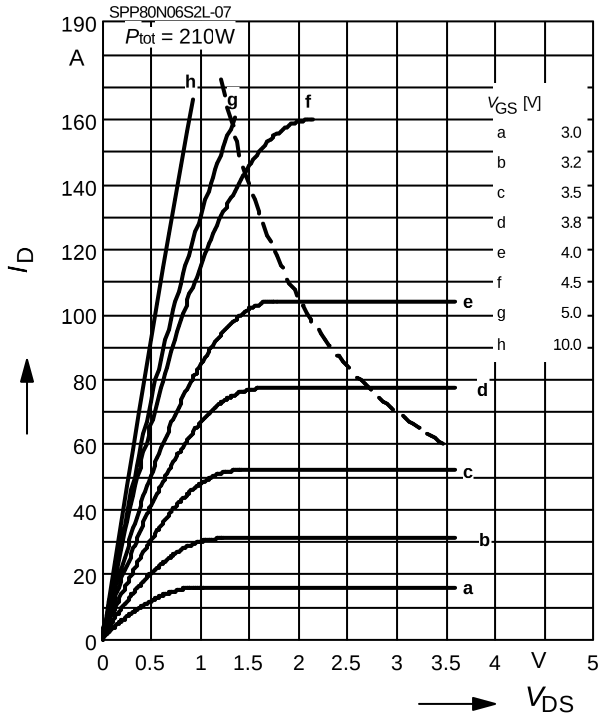
parameter : $D = t_p/T$



5 Typ. output characteristic

$I_D = f(V_{DS})$; T_j=25°C

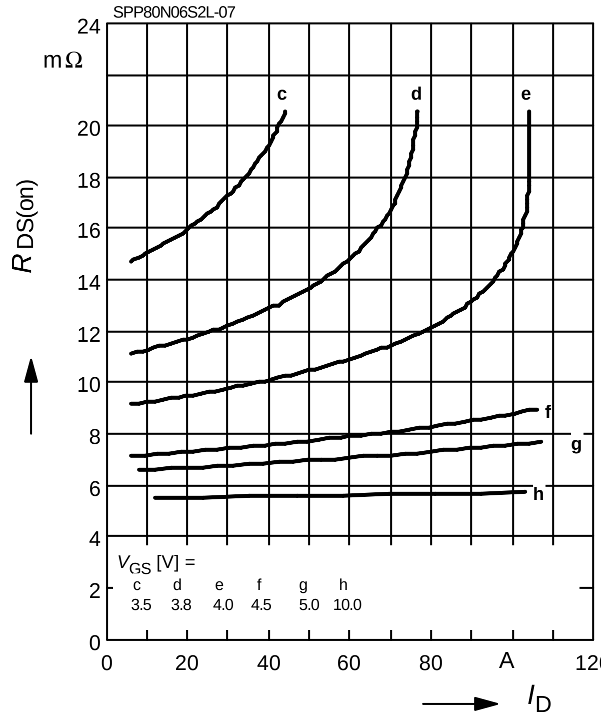
parameter: t_p = 80 µs



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D)$

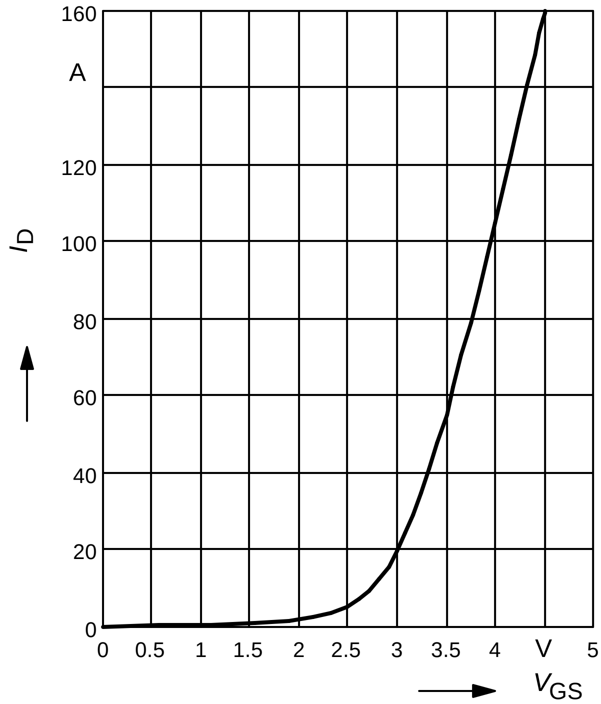
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

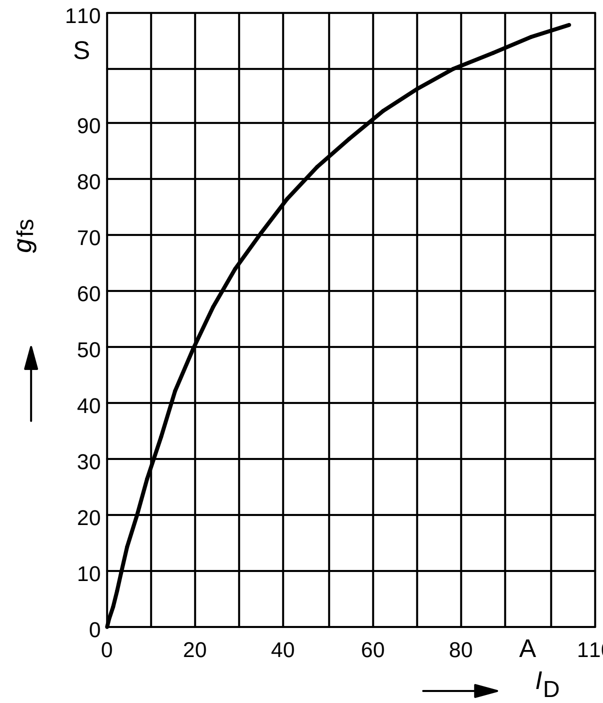
parameter: t_p = 80 µs



8 Typ. forward transconductance

$g_{fs} = f(I_D)$; T_j=25°C

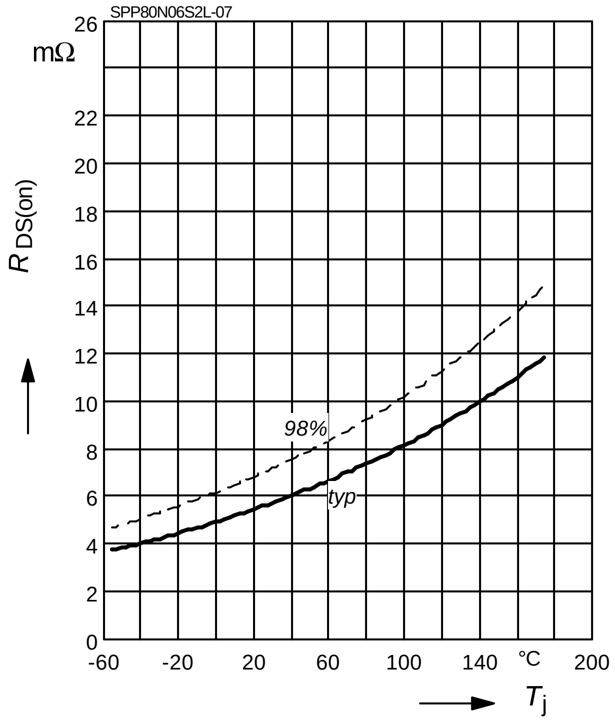
parameter: g_{fs}



9 Drain-source on-state resistance

$R_{DS(on)} = f(T_j)$

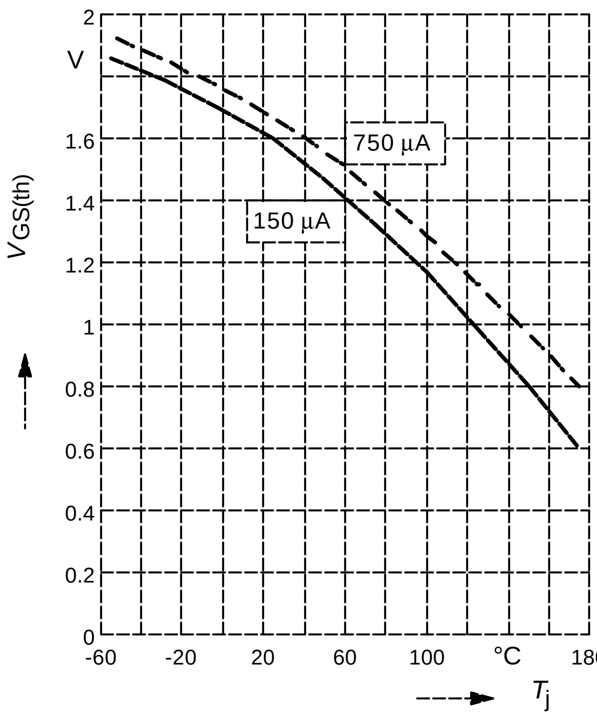
parameter : I_D = 60 A, V_{GS} = 10 V



10 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$

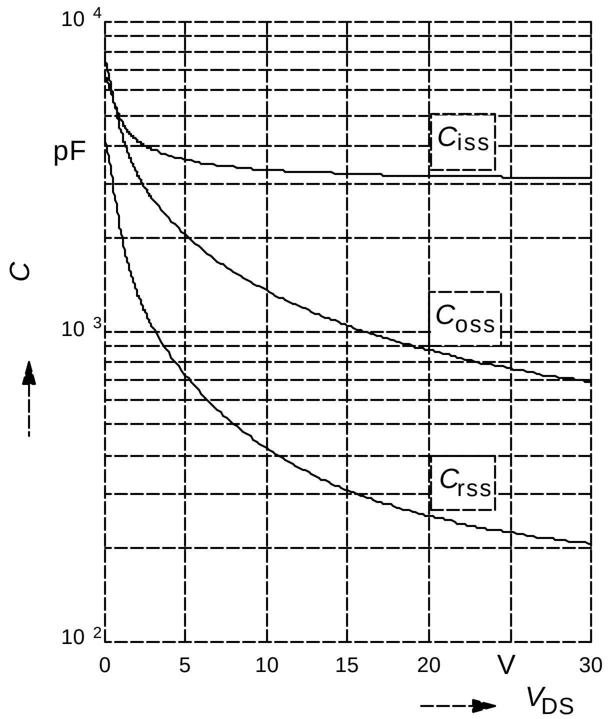
parameter: $V_{GS} = V_{DS}$



11 Typ. capacitances

$C = f(V_{DS})$

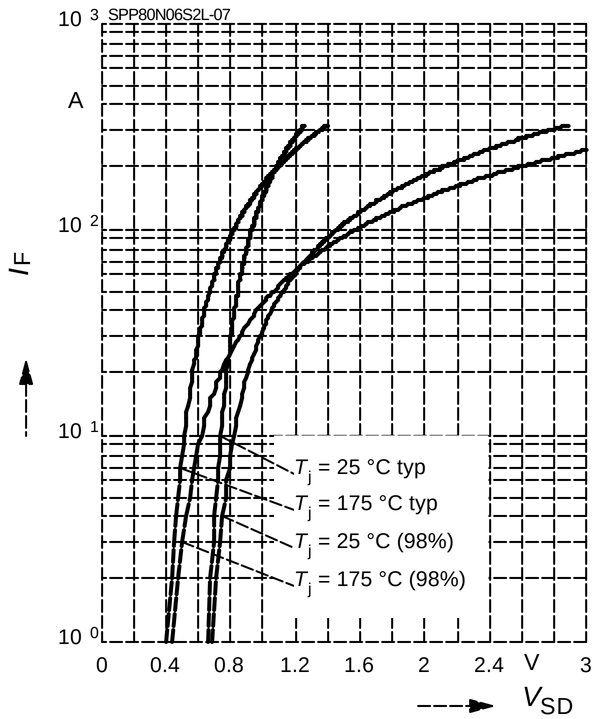
parameter: V_{GS}=0V, f=1 MHz



12 Forward character. of reverse diode

$I_F = f(V_{SD})$

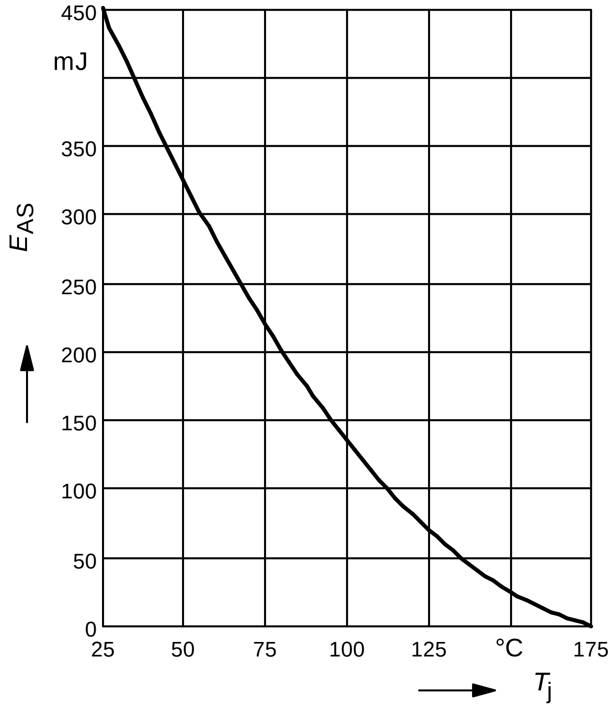
parameter: T_j , t_p = 80 µs



13 Typ. avalanche energy

$E_{AS} = f(T_j)$

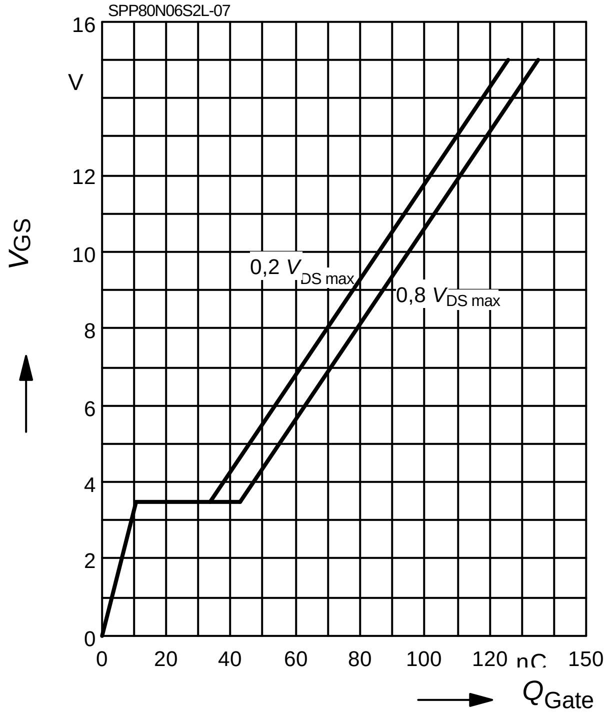
par.: I_D = 80 A , V_{DD} = 25 V, R_{GS} = 25 Ω



14 Typ. gate charge

$V_{GS} = f(Q_{Gate})$

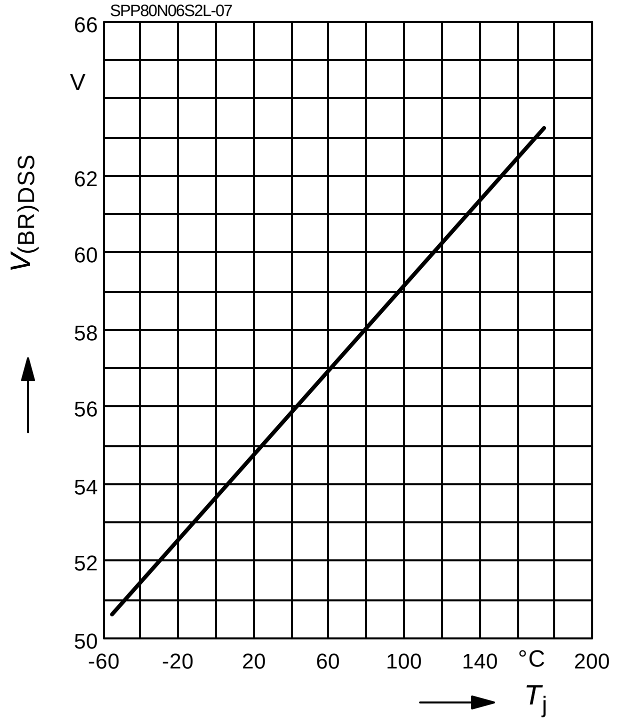
parameter: I_D = 80 A pulsed



15 Drain-source breakdown voltage

$V_{(BR)DSS} = f(T_j)$

parameter: I_D=10 mA



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Further information
Please notice that the part number is **B**SPP80N06S2L-07 and **B**SPB80N06S2L-07, for simplicity the device is referred to by the term SPP80N06S2L-07 and SPB80N06S2L-07 throughout this documentation.